AMENDMENTS TO THE SPECIFICATION:

Substitute the following amendment to paragraph 0006 showing changes for paragraph 0006, page 3 in the application: .

[0006] Figure 1 is a plan view illustrating a prior art FET formed in a SOI substrate, the FET having a body contact. Figure 1 illustrates a FET having two fingers 102 which extend in a direction of the length 115 of an active area 110. The two fingers are placed parallel to each other, dividing the width 120 of the active area 110 into three parts, the two sources 113 provided between the fingers 102 ~~110~~ and the outer edges of the active area 110 and the drain 114 provided between the two fingers 102. The two-finger design is advantageous because it provides increased current drive over a one-finger FET design occupying an active area of the substrate having the width 120.

Substitute the following amendment to paragraph 0031 showing changes for paragraph 0031, beginning on page 9 in the application:

[0031] Figures 7A through 15 illustrate a method of fabricating the FET shown in Figures 5 and 6. Figure 7A is a cross-sectional view of a silicon-on-insulator (SOI) substrate 750. As shown in Figure 7A, an active area 700 of the SOI substrate includes a relatively thin layer 743 of a single-crystal semiconductor overlying a buried oxide (BOX) layer 742, which in turn, overlies a bulk portion 742 of the substrate 750. Such silicon-on-insulator (SOI) substrate is an example of semiconductor-on-insulator substrates which can include any one of several semiconductor materials other than silicon as the material of the upper single-crystal layer and the bulk portion 742 ~~740~~. Isolation structures such as trench isolations 760 are further provided, which bound the active area 700. Figure 7B is a top down view of the SOI substrate shown in Figure 7A. Active area 700 is the area between isolation structures 760. In an embodiment, the

isolation structures 760 bound the active area 700 on all sides. However, in another embodiment, the isolation structures bound the active area 700 only on two sides, such as those shown at the top edge 710 and bottom edge 712 of Figure 7B, leaving the left side 720 and the right side 722 of the active area 700 non-isolated as common regions between the sources of FETs that are disposed in side-to-side relation with each other.